**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An integrated semiconductor device, comprising:

a semiconductor material substrate;

a polysilicon line, said polysilicon line having micro-rough indentations on a top surface portion of the polysilicon line formed by chemical mechanical polishing using a slurry solution having particles of a maximum size of less than one-half of a width of the polysilicon line; and

a silicide film covering said micro-rough top surface portion of the polysilicon line.

2. (Original) The integrated device of claim 1, further comprising:

a plurality of isolation areas;

a thin oxide film between said polysilicon line and the substrate; and

a plurality of patterned active regions positioned on the substrate and on opposite sides of said polysilicon line.

3. (Original) The integrated device of claim 2 wherein said polysilicon line forms a polysilicon gate region of the device and said active regions are source and drain regions of the device.

4. (Original) The integrated device of claim 3, further comprising spacers adjacent to the polysilicon gate region and lightly doped regions under said spacers and adjacent to said source and drain regions.

5. (Original) The integrated device of claim 1 wherein said silicide film comprises titanium silicide or titanium silicide/titanium nitride stack film.

6. (Original) The integrated device of claim 1 wherein said silicide film covering said micro-rough top surface of the polysilicon line has an increased effective surface area.

7. (Original) The integrated device of claim 1, further comprising a metallization structure positioned on the silicide film for providing interconnection.

8. (Original) The integrated device of claim 7 wherein said metallization structure comprises a multi-stack metal layer.

9. (New) The integrated device of claim 1 wherein the width of the polysilicon line is less than 0.1 μm.

10. (New) The integrated device of claim 1 wherein the silicide film is formed to not enter a C-54 transformation phase.

11. (New) The integrated device of claim 1 wherein the silicide film is formed to enter a C-49 phase and not a C-54 phase.

12. (New) An integrated circuit, comprising:

a polysilicon line formed to have micro-rough indentations on a top surface by chemical mechanical polishing using a slurry solution having particles of a maximum size of less than one-half of a width of the polysilicon line; and

a silicide formed on the micro-rough top surface of the polysilicon line without entering a C-54 transformation phase.

13. (New) The integrated circuit of claim 12 wherein the silicide film is formed to enter a C-49 phase without entering the C-54 phase.

14. (New) The integrated circuit of claim 12 wherein the polysilicon line is less than 0.1 μm in width.

15. (New) A semiconductor device, comprising:

a polysilicon line formed on a semiconductor material substrate, the polysilicon line having a width no greater than 0.1 μm and a top surface treated by chemical mechanical polishing using a slurry solution having particles of a maximum size of less than one-half the width of the polysilicon line to form micro-rough indentations in the top surface; and

a silicide film formed on the micro-rough top surface of the polysilicon line.

16. (New) The device of claim 15 wherein the silicide film is formed to not enter a C-54 transformation phase.

17. (New) The device of claim 16 wherein the silicide film is formed to enter a C-49 phase without entering the C-54 phase.

18. (New) The device of claim 17, further comprising a metallization structure positioned on the silicide film for providing interconnection.

19. (New) The device of claim 18 wherein the metallization structure comprises a multi-stack metal layer.

20. (New) The device of claim 17 wherein the silicide film comprises titanium silicide or titanium silicide/titanium nitride stack film.